EL979955196

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No	10/241,923
Priority Filing Date	September 11, 2002
Inventor	David L. Dickerson et al.
Assignee	Micron Technology, Inc.
Priority Group Art Unit	2814
Priority Examiner	A.D. Mai
Attorney's Docket No	MI22-2500
Title: Isolation Region Forming Methods	

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INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, copending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 10/241,923, filed September 11, 2002, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, Applicant submits copies of the cited foreign references and articles (ONLY) for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 3 - (1 - 04)

D. Brent Kenady Reg. No. 40,045

Sheet 1 of 4 Form PTO-1449 U.S. DEPARTMENT OF COMMERCE ATTY. DOCKET NO. SERIAL NO. PATENT AND TRADEMARK OFFICE MI22-2500 Filed Herewith APPLICANT LIST OF ART CITED BY APPLICANT David L. Dickerson et al. (Use several sheets if necessary) FILING DATE GROUP Filed Herewith Unknown U.S. PATENT DOCUMENTS *Examiner Document Date Name Class Subclass Filing Date Initial Number If Appropriate AA5,674,775 10/7/97 Ho et al. ΑB 6,040,232 3/21/00 Gau AC 6,074,932 6/13/00 Wu AD 6,090,684 7/18/00 Ishitsuka et al. AE 6.093.621 7/25/00 Tseng ΑF 6,103,635 8/15/00 Chau et al. AG 6,153,480 11/28/00 Arghavani et al. ΑH 5,981,356 11/99 Hsueh et al. ΑI 5,989,975 11/99 Kuo ΑJ 6,153,478 11/00 Lin et al. 6,232,203 B1 05/01 ΑK Huang 6,249,035 B1 06/01 Peidous et al. AL FOREIGN PATENT DOCUMENTS Document Date Country Class Subclass Number Yes No EP 0 782 185 A2 02.07.97 AM Europe (NEC Corporation) AN JP 11-67890 Japan JP 2000-269318 9/29/00 AO Japan х ΑP OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)Q AR IBM Corp., Optimized Shallow Trench Isolation Structure and Its Process for Eliminating Shallow Trench Isolation-Induced Parasitic Effects, 34 IBM Technical Disclosure Bulletin, No. 11, pp. 276-277 (April 1992). AR Texas Instruments SPIE, Vol. 2875, A Study of Integration Issues in Shallow Trench Isolation for Deep Submicron CMOS Technologies,

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Form PTO-1449 U.S. DEPARTMENT OF COMMERCE ATTY. DOCKET NO. SERIAL NO. PATENT AND TRADEMARK OFFICE M122-2500 Filed Herewith LIST OF ART CITED BY APPLICANT APPLICANT David L. Dickerson et al. (Use several sheets if necessary) FILING DATE GROUP Filed Herewith Unknown U.S. PATENT DOCUMENTS *Examiner Class Subclass Filing Date Document Date Name Initial Number If Appropriate 4,663,832 05/12/87 Jambotkar ΑB 5,677,233 10/14/97 Abiko 5,712,185 AC 01/27/98 Tsai et al. AD 5,780,346 07/14/98 Arghavani et al. 09/01/98 ΑE 5,801,083 Yu et al. 5,895,254 ΑF 04/20/99 Huang et al. AG 5,397,733 3/14/95 Jang ΑH 5,728,620 3/17/98 Park 5,904,538 05/18/99 ΑI Son et al. AJ 5,966,614 10/12/99 Park et al. 6,083,808 7/4/00 Shin et al. ΑK 5,863,827 01/26/99 ΑL Joyner FOREIGN PATENT DOCUMENTS Date Country Class Subclass Translation Number No Yes AM AN AΟ ΑP OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) AR S. Wolf et al., Silicon Processing for the VLSI Era, Vol. 1, pages 522, 534, and 541; 1986. AS K. Ishimaru et al., Trench Isolation Technology with 1 Micron Depth n-and p-Wells for a Full CMOS SRAM Cell with a 0.4 Micron. . . . IEEE 1994 pps. 97-98 ΑT Fazan & Mathews, "A Highly Manufacturable Trench Isolation Process for Deep Submicron DRAMs," IEEE 1993, 4 pages. EXAMINER DATE CONSIDERED

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